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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,554	DORSEY, MICHAEL C.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to applicant's amendment filed 6/4/2004, wherein Claim 7 was canceled.

Claims 1-6 and 8-37 are pending in this action.

Response to Amendment

The examiner acknowledges and approves the applicant's changes to the Drawings and Disclosure.

Re: Claim Rejections

1. Applicant's arguments based on the amendment filed 6/4/2004, with respect to the rejection(s)of claim(s) 1-6 and 8-37 under 35 USC § 112(1) and 112(2), 102(b), and 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of the addition of the following limitation to the independent claims: "wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit".

Claim Rejections - 35 USC § 103

2. Claims 1, 6, 13, 15, 18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Kohno, U.S. Patent No. 5943285.

As per Claims 1 and 13:

Motika et al. teaches a dual mode built-in self-test controller (FIG.2 and column 4 lines 5-7), comprising: a logic built-in self-test domain (FIG.2 34, 38), including: a logic built-in self-test engine/means capable of executing a logic built-in self-test (FIG.2 34); and a logic built-in self-test signature/storage means generated by an execution of the logic built-in self-test (column 3 lines39-67 and column 4 lines 1-5); and a memory built-in self-test domain (FIG.2 32, 36), including: a memory built-in self-test engine/means capable of executing a memory built-in self-test (FIG.2 32). Not taught by Motika is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 27 lines 21-29. And in column 1 lines 6-9 and column 5 lines 57-67, the inventor cites advantages of less restricted design requirements while maintaining fast circuit speed. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to apply the centralized theme of Kohno to the controller taught by Motika et al. in order to produce a better self-testing product.

As per Claims 6 and 15:

Motika et al. further teaches the dual mode built-in self-test controller of claim 1 and 13, wherein the memory built-in self-test domain (FIG.2 32, 36) further comprises a memory built-in self-test signature/storage means generated by an execution of the memory built-in self-test (column 3 lines 39-63). And in view of the motivation previously stated, the claims are rejected.

As per Claim 18:

Motika et al. teaches an integrated circuit device (column 1 lines 5-8), comprising: a plurality of memory components (FIG.2 36); a logic core (FIG.2 38); a testing interface (FIG.2 60); and a dual mode built-in self-test controller (FIG.2 50) controlled through the testing interface, comprising: a logic built-in self-test domain (FIG.2 34, 38), including: a logic built-in self-test engine (FIG.2 34) capable of executing a logic built-in self-test on the logic core (column 3 lines 64-67 and column 4 lines 1-5); and a logic built-in self-test signature generated by an execution of the logic built-in self-test (column 3 lines 38-67 and column 4 lines 1-5); and a memory built-in self-test domain (FIG.2 32, 36), including: a memory built-in self-test engine (FIG.2 32) capable of executing a memory built-in self-test on the memory components (FIG.2 36). Not taught by Motika is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 27 lines 21-29. And in column 1 lines 6-9 and column 5 lines 57-67, the inventor cites advantages of less restricted design requirements while maintaining fast circuit speed. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to apply the centralized theme of Kohno to the controller taught by Motika et al. in order to produce a better self-testing product.

As per Claim 20:

Motika et al. further teaches the integrated circuit device of claim 18, wherein the memory built-in self-test domain (FIG.2 32, 36) further comprises a memory built-in self-test signature register generated by an execution of the memory built-in self-test

(column 3 lines 41-63). And in view of the motivation previously stated, the claim is rejected.

3. Claims 2, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189 and Kohno, U.S. Patent No. 5943285, as applied to Claim 1, 13 and 18 above, and further in view of Koproski et al., U.S. Patent No. 6671838. The claims are dependent on Claim 1, 13 or 18 above, and limit the LBIST to comprise an LBIST state machine and pattern generator. In an analogous art, Koproski et al., in column 3 lines 1-5 teaches a state machine for an LBIST device, and, in FIG.1, Koproski et al. teaches a pattern generator 4. And in column 1 lines 1-67 and column 2 lines 1-28, the reference states the advantage of using a special analysis system for creating weighted patterns for testing in an LBIST. One with ordinary skill in the art at the time of the invention, motivated by Koproski et al., would combine the references, and so the claims are rejected.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, in view of Koproski et al., U.S. Patent No. 6671838 as applied to Claim 2, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997. The LBIST state machine in Claim 2 is further limited to a reset state entered via an external signal. Zuraski et al. enters a state via an external reset signal (Zuraski et al, column 10 lines 31-36), but does not begin initializing the device with an LBIST run signal. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the

same chip (column 6 lines 9-12). And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. And Zuraski Jr. et al., professes the advantages (column 2 lines 10-18) of a readily programmable BIST that would not need constant revision as needs change. In view of the motivations for Zuraski et al. and Lo et al., and in view of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claim is rejected.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, in view of Koproski et al., U.S. Patent No. 6671838 as applied to Claim 2, and further in view of Rajski et al., U.S. Patent No. 6684358. The controller of Claim 2 is limited wherein the pattern generator is an LFSR seeded with a primitive polynomial. In an analogous art, Rajski et al., in column 8 lines 6-9 teaches such pattern generator. In column 2 lines 15-33, the Rajski et al. recites an improved pattern generator that allows fuller test coverage than predecessors. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Rajski et al., would combine the references, and so the claim is rejected.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, in view of Koproski et

al., U.S. Patent No. 6671838 as applied to Claim 2, in view of Hong-Shin Jun, U.S. Patent No. 6658611, and further in view of Au et al., U.S. Patent No. 6681359. The controller of Claim 2 is limited wherein the signature includes an error bit (Jun column 5 lines 43-63) and a "done" bit (Au et al. column 9 lines 25-33). Jun cites an improved programmable BIST using optimum test patterns (column 2 lines 10-13), and Au et al. cites control of BIST using a standard interface (column 2 lines 18-26). And one with ordinary skill in the art at the time of the invention, motivated as suggested above, would combine the references, and therefore the claim is rejected.

7. Claims 8 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189 and Kohno, U.S. Patent No. 5943285 as applied to Claim 6 and 18 above, and further in view of Au et al., U.S. Patent No. 6681359.

As per Claim 8:

In a similar art, Au et al. teaches the signature register as containing a test done bit in column 9 lines 25-33, and based on the motivation for Au et al. stated elsewhere, the claim is rejected.

As per Claim 24:

The integrated circuit device of claim 18 is limited wherein testing interface comprises a Joint Test Action Group tap controller. Au et al., in the Abstract teaches this feature, and in view of the motivation stated elsewhere, the claim is rejected.

8. Claims 9, 11 and 16, 17, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, and in view of Zuraski Jr. et al., U.S. Patent No. 6560740. Dependent on

Claim 1 or 13 or 18, Claims 9 or 21 limit the MBIST engine to comprise a MBIST state machine and Claim 11 or 17 or 22 limit to a plurality of state machines, whereas Claims 16 and 17 are based on a means, and a nested MBIST engine driving a state machine. In an analogous art, Zuraski Jr. et al. teaches the same hierarchy where an MBIST state machine(s) (FIG.1 20a, 20b) is/are driven by an MBIST engine (FIG.1 18) as is described in column 5 lines 40-54. And Zuraski Jr. et al., professes the advantages (column 2 lines 10-18) of a readily programmable BIST that would not need constant revision as needs change. One with ordinary skill in the art at the time of the invention, motivated as suggested by Zuraski Jr. et al., would combine the references, and so the claims are rejected.

9. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, and in view of Zuraski Jr. et al., U.S. Patent No. 6560740 as applied to Claim 9 and 11 above, and further in view of Lo et al., U.S. Patent No. 5661732. The claims further limit the controller wherein the state machine comprises a reset state entered upon an external reset signal (Zuraski et al, column 10 lines 31-36). However Zuraski et al. does not further limit the machine to flushing and testing. In an analogous art, Lo et al., upon entering a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state produces internal resets of registers, and then as a programmable option, a flush of the memory may occur (column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (FIG.1 26). In Lo et al. column

2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. One with ordinary skill in the art at the time of the invention, motivated by Lo et al., would combine the references, and so the claims are rejected.

10. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, and in view of Kim et al., U.S. Patent No. 6148426. The integrated circuit device of claim 18 is limited wherein the memory components include a static random access memory device. In an analogous art, Kim et al. performs MBIST operations on an SRAM (see Title). And as Kim et al. in column 1 lines 43-45 states as an advantage to be a smaller address generator, one with ordinary skill in the art at the time of the invention, motivated by Kim et al., would combine the references, and thus the claim is rejected.

11. Claims 25, 26, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, and in view of Kraus et al., U.S. Patent No. 6587979.

As per Claim 25:

Motika et al. teaches a method for performing a BIST using a dual-mode controller (FIG.2 50). Not taught by Motika is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 27 lines 21-29. And in column 1 lines 6-9 and column 5 lines 57-67, the inventor cites advantages of less restricted design requirements while maintaining fast circuit speed. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious

to apply the centralized theme of Kohno to the controller taught by Motika et al. in order to produce a better self-testing product. Also, Motika et al. does not specify that the controller be reset externally. However, in an analogous art, the MBIST of Kraus et al., resets the MBIST controller of FIG.7 by way of the tester 21 (column 9 lines 52-58), and performs an MBIST (column 15 lines 24-35), and obtaining results (column 8 lines 10-36) of the MBIST. Column 2 lines 32-40 of Kraus et al. explains the attributes of the invention as being a highly adaptable and flexible platform for testing memories, and one with ordinary skill in the art at the time of the invention, motivated by Kraus et al., would combine the references, as so the claim is rejected.

As per Claim 26:

Dependent on Claim 25, the claim limits the reset of the controller includes resetting the MBIST engine. Kraus et al., shows the path of the reset signal from the JTAG bus to the core wrapper (FIG.6) pattern generator, which is part of the MBIST engine. And in view of the motivation previously stated for Kraus et al., the claim is rejected.

As per Claim 31:

The claim limits Claim 25 in that the signature register of Motika et al. includes storing results of the built-in self-test (see column 3 lines 39-63). And in view of the motivation previously stated, the claim is rejected.

12. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, and in view of Kraus et al., U.S. Patent No. 6587979 as applied to Claim 25, and further in view of Rajski et

al., U.S. Patent No. 6684358. Dependent on Claim 25, the claim limits resetting a MISR and a pattern generator in an LBIST. Rajski et al. performs these functions on an LBIST (column 4 lines 10-57), and in view of the motivation for Rajski et al. previously stated, the claim is rejected.

13. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, and in view of Kraus et al., U.S. Patent No. 6587979 as applied to Claim 25, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997.

As per Claim 28:

The BIST state machine in Claim 25 is further limited to a reset state entered via an external signal. Zuraski et al. enters a state via an external reset signal (Zuraski et al, column 10 lines 31-36), but does not begin initializing the device with an LBIST run signal. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the same chip (column 6 lines 9-12). And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. And Zuraski Jr. et al., professes the advantages (column 2 lines 10-18) of a readily programmable BIST that would not need constant revision as needs change. In view of

the motivations for Zuraski et al. and Lo et al., and in view of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claim is rejected.

As per Claim 30:

The claim further limits the method wherein the state machine comprises a reset state entered upon an external reset signal (Zuraski et al, column 10 lines 31-36). However Zuraski et al. does not further limit the method to flushing and testing. In an analogous art, Lo et al., upon entering a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state produces internal resets of registers, and then as a programmable option, a flush of the memory may occur (column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (FIG.1 26). In Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. One with ordinary skill in the art at the time of the invention, motivated by Lo et al., would combine the references, and so the claim is rejected.

14. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, Kohno, U.S. Patent No. 5943285, and in view of Kraus et al., U.S. Patent No. 6587979 as applied to Claim 25,, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997 as applied to Claim 28, in view of Hong-Shin Jun, U.S. Patent No. 6658611, and further in view of Au et al., U.S. Patent No. 6681359. The method of

Claim 28 is limited wherein the signature (MISR) includes an error bit (Jun column 5 lines 43-63) and a "done" bit (Au et al. column 9 lines 25-33). Jun cites an improved programmable BIST using optimum test patterns (column 2 lines 10-13), and one with ordinary skill in the art at the time of the invention, motivated as suggested above and previously for Au et al., would combine the references, and therefore the claim is rejected.

15. Claim 32, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, Kohno, U.S. Patent No. 5943285, and in view of Motika et al., U.S. Patent No. 5982189.

As per Claim 32:

Au et al. teaches a method for testing an integrated circuit device (see Abstract), the method comprising: interfacing the integrated circuit device with a tester (column 7 lines 31-34 and column 8 lines 29-31); and Zuraski et al. enters a state via an external reset signal (Zuraski et al, column 10 lines 31-36), performing a logic built-in self-test (Motika et al. column 3 lines 64-66), performing a memory built-in self-test (Motika et al. column 3 lines 39-43), and obtaining the results of the LBIST and MBIST (Motika et al. column 3 lines 55-60 and column 4 lines 1-3). Not taught by Motika is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 27 lines 21-29. And in column 1 lines 6-9 and column 5 lines 57-67, the inventor cites advantages of less restricted design requirements while maintaining fast circuit speed.

One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to apply the centralized theme of Kohno to the controller taught by Motika et al. in order to produce a better self-testing product.

As per Claim 36:

Au et al. teaches the method of claim 32, and obtaining the results by reading the signature (column 10 lines 21-26). And in view of the previously stated motivation, the claim is rejected.

As per Claim 37:

Au et al. teaches the method of claim 32, wherein interfacing the integrated circuit device with the tester includes employing Joint Test Action Group protocols (column 10 lines 21-25). And in view of the previously stated motivation, the claim is rejected.

16. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, Kohno, U.S. Patent No. 5943285, and in view of Motika et al., U.S. Patent No. 5982189 as applied to Claim 32 above, and further in view of Kraus et al., U.S. Patent No. 6587979. Motika et al. teaches a method for performing a BIST using a dual-mode controller (FIG.2 50), but does not specify that the controller be reset. However, in an analogous art, the MBIST of Kraus et al., resets the MBIST controller of FIG.7 by way of the tester 21 (column 9 lines 52-58), and in view of the motivation previously stated, the claim is rejected.

17. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, Kohno, U.S. Patent No. 5943285, and in view of Motika et al., U.S. Patent No. 5982189 as applied to Claim 32 above, and further in view of Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the same chip (column 6 lines 9-12). And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. In view of the elsewhere stated motivations for Lo et al., and of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claim is rejected.

18. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., Kohno, U.S. Patent No. 5943285, U.S. Patent No. 6560740, and in view of Motika et al., U.S. Patent No. 5982189 as applied to Claim 32 above, and further in view of Lo et al., U.S. Patent No. 5661732. In an analogous art, Lo et al., upon enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state producing internal resets of registers, and then as a programmable option, a flush of the memory may occur (column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done

signal (FIG.1 26). In Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. One with ordinary skill in the art at the time of the invention, motivated by Lo et al., would combine the references, and so the claim is rejected.

In total, the Claims 1-6 and 8-37 are therefore rejected.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-

0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Guy J. LAMARRE
PRIMARY EXAMINER